CLAIMS

1. An integrated circuit on a monocrystalline substrate, the integrated circuit comprising:

a matrix of non-volatile memory cells, each non-volatile floating memory cell having a floating gate and a control gate, both gates being electroconductive, and an intermediate dielectric multilayer disposed between the floating gate and control gate for electrically insulating the floating gate and the control gate from one another, the intermediate dielectric multilayer including at least a first silicon oxide layer; and

at least one first and one second transistor type formed in zones of the substrate peripheral to the matrix of non-volatile memory cells and having multilayer gate dielectrics of a first and second thickness, respectively, wherein the multilayer gate dielectric of both the first type and the second type of peripheral transistors include a second silicon oxide layer formed by means of a thermal treatment, and a third silicon oxide layer overlying the second silicon oxide layer, the third silicon oxide layer being densified by said thermal treatment.

2. The integrated circuit of claim 1, wherein said third silicon oxide layer and said first silicon oxide layer of the intermediate dielectric multilayer are the same layer.

3. The integrated circuit of claim 1, wherein said transistors of the first and the second type are high voltage and low voltage transistors, respectively, and said second thickness of the gate dielectric of the second transistor type is less than said first thickness of the gate dielectric of the first transistor type.

4. The integrated circuit of claim 1, wherein the thickness of said multilayer gate dielectric of said second transistor type is less than that of said multilayer gate dielectric of said first transistor type.

5. The integrated circuit of claim 1, wherein the multilayer gate dielectrics of the first and second types are nitridized to increase the quality and reliability of the gate dielectrics.

6. The integrated circuit of claim 1, wherein the thickness of said first silicon oxide layer is between 50Å and 250Å and said first thickness and said second thickness of the gate dielectrics

are between 70Å and 350Å.

7. An integrated circuit comprising:

a substrate;

at least one memory cell formed in the substrate, the memory cell having a floating gate, a control gate, and a multilayer dielectric disposed on the floating gate and the control gate and including a deposited layer, the multilayer dielectric insulating the floating gate from the control gate;

a first transistor formed in the substrate in a first area of the substrate peripheral to the at least one memory cell, the first transistor having a gate dielectric comprising:

the deposited layer;

a first layer underlying the deposited layer of the first transistor, formed by thermal oxidation of the substrate; and

a second layer underlying the deposited layer of the first transistor, formed by thermal oxidation of the substrate; and

a second transistor formed in the substrate in a second area of the substrate peripheral to the at least one memory cell, the second transistor having a gate dielectric comprising:

the deposited layer; and

a first layer underlying the deposited layer of the second transistor, formed by thermal oxidation of the substrate.

8. The integrated circuit of claim 7, wherein the at least one memory cell and the first and second transistors are MOS transistors.

9. The integrated circuit of claim 7, wherein the first layer underlying the deposited layer of the first transistor and the first layer underlying the deposited layer of the second transistor are different regions of the same layer, the layer being formed on the surface of the substrate.